EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1915	phase shift AND clock AND ("FIFO" OR first in first out) AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/24 08:04
L2	1531	error AND phase shift AND clock AND ("FIFO" OR first in first out) AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/24 08:05
L4	95	interpolator AND (jitter OR noise) AND error AND phase shift AND clock AND ("FIFO" OR first in first out) AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/24 08:08
L5	1	("BIST" OR built-in self-test OR built in self test) AND interpolator AND (jitter OR noise) AND error AND phase shift AND clock AND ("FIFO" OR first in first out) AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/24 08:08
L6	459	(underflow OR overflow) AND (jitter OR noise) AND error AND phase shift AND clock AND ("FIFO" OR first in first out) AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/24 08:09
L7	235	reference clock AND (underflow OR overflow) AND (jitter OR noise) AND error AND phase shift AND clock AND ("FIFO" OR first in first out) AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/24 08:09
L8	235	signal AND reference clock AND (underflow OR overflow) AND (jitter OR noise) AND error AND phase shift AND clock AND ("FIFO" OR first in first out) AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/24 08:12
L9	3	interpolator AND signal AND reference clock AND (underflow OR overflow) AND (jitter OR noise) AND error AND phase shift AND clock AND ("FIFO" OR first in first out) AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/24 08:12

EAST Search History

L11	2	"7093172".pn.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/24 08:18
S1	491	713/194.ccls. AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 10:36
S2	2	"6397042".pn.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/20 17:54
S3	2	"6433599".pn.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/20 17:55
S4	2	"6768433".pn.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/20 17:55
S5	2	"6826495".pn.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/20 17:55
S6	0	test signal AND jitter AND clock AND serialization AND 713/194.ccls. AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 10:36
S7	48	test signal AND jitter AND clock AND serialization AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 10:37

EAST Search History

S8	41	data recovery AND test signal AND jitter AND clock AND serialization AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 10:37
S9	0	controled AND data recovery AND test signal AND jitter AND clock AND serialization AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 10:37
S10	41	sequence AND data recovery AND test signal AND jitter AND clock AND serialization AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 10:37
S11	41	signal AND sequence AND data recovery AND test signal AND jitter AND clock AND serialization AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 11:20
S12	9	signal AND sequence AND data recovery AND test signal AND jitter AND clock AND serialization AND ("380".clas. OR "713". clas. OR "726".clas.) AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 10:38
S13	0	serial transceiver AND signal AND sequence AND data recovery AND test signal AND jitter AND clock AND serialization AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 14:12
S14	67	signal AND data recovery AND test AND jitter AND clock AND serialization AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 14:12
S15	0	signal AND data recovery AND test AND jitter AND serialization clock AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 14:12

EAST Search History

S16	13	serialization clock AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 14:13
S17	4	jitter AND serialization clock AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 14:21
S18	4	signal recovery AND testing AND test signal AND serial AND jitter AND clock AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 14:26
S19	118	(test OR testing) AND test signal AND (serialication OR serialized) AND (jitter OR noise) AND clock AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 14:29
S20	0	(test OR testing) AND test signal AND (serialication OR serialized) AND (jitter OR noise) AND clock AND (257/922.ccls.) (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 14:28
S21	0	(test OR testing) AND test signal AND (serialication OR serialized) AND (jitter OR noise) AND clock AND ("257".clas.) (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 14:28
S22	82	transceiver AND (compensat$3 OR tolerat$3) AND (test OR testing) AND test signal AND (serialization OR serialized) AND (jitter OR noise) AND clock AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 14:31
S23	143	(compensat$3 OR tolerat$3) AND (test OR testing) AND test signal AND (serialization OR serialized) AND (jitter OR noise) AND clock AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 14:31

EAST Search History

S24	0	serial transceiver AND (compensat$3 OR tolerat$3) AND (test OR testing) AND test signal AND (serialization OR serialized) AND (jitter OR noise) AND clock AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 14:32
S25	125	(transceiver OR transmitter OR receiver) AND serial AND (compensat$3 OR tolerat$3) AND (test OR testing) AND test signal AND (serialization OR serialized) AND (jitter OR noise) AND clock AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 14:32
S26	134	serial AND (compensat$3 OR tolerat$3) AND (test OR testing) AND test signal AND (serialization OR serialized) AND (jitter OR noise) AND clock AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 14:33
S27	129	(compar$3) AND serial AND (compensat$3 OR tolerat$3) AND (test OR testing) AND test signal AND (serialization OR serialized) AND (jitter OR noise) AND clock AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 14:33
S28	125	sequence AND (compar$3) AND serial AND (compensat$3 OR tolerat$3) AND (test OR testing) AND test signal AND (serialization OR serialized) AND (jitter OR noise) AND clock AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 14:34
S29	6	interpolator AND sequence AND (compar$3) AND serial AND (compensat$3 OR tolerat$3) AND (test OR testing) AND test signal AND (serialization OR serialized) AND (jitter OR noise) AND clock AND (@pd<"20040225" or @ad<"20040225" or @prad<"20040225" or @rlad<"20040225")	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/24 08:03
S30	2	"20010016929".pn.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 15:02
S31	2	"5835501".pn.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 15:17

EAST Search History

S32	2	"5802073".pn.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 15:18
S33	2	"5418789".pn.	US-PGPUB; USPAT; USOCR; EPO; DERWENT; IBM_TDB	ADJ	ON	2007/09/21 16:00

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serialization clock jitter test signal | Search Patents | Advanced Patent Sear | Google Patent Search

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Patents

Patents **1 - 18** on **serialization clock jitter test signal**. (**0.08** seconds)

Sort by relevance | Sort by date (new first) | Sort by date (old first)

Built-in self **test** system and method for high speed **clock** and data recovery ...

US Pat. 6834367 - Filed Dec 21, 2000 - International Business Machines Corporation
The **clock** and data recovery circuit derives the **clock signal** from the received digital ... The **test** is comprised of the steps of generating a **jitter clock**, ...

Multi level **jitter** pre-compensation logic circuit for high speed data links

US Pat. 6384661 - Filed May 30, 2000 - International Business Machines Corporation
Also, the input **test signal** is sent to the I input of ... through said said forth section to compensate the **serialization** of the third section for **jitter**. ...

Self **test** of an electronic device

US Pat. 6397042 - Filed Mar 2, 1999 - Texas Instruments Incorporated
If transmit data is 15 supplied relative to the reference **clock**, at 43, ...
circuit device comprising: a **clock** source, having an output for a **clock signal**; ...

Method for distributing sets of collision resolution parameters in a frame ...

US Pat. 6877043 - Filed Apr 4, 2001 - Broadcom Corporation
If a **jitter clock** is used for the sampling of the input **signal**, ... frame on an HPNA V2 network has three major components: **serialization** delay (the time it ...

Method of providing synchronous transport of packets between asynchronous ...

US Pat. 7000031 - Filed Apr 4, 2001 - Broadcom Corporation
If a **jitter clock** is used for the sampling of the input **signal**, ... frame on an HPNA V2 network has three major components: **serialization** delay (the time it ...

Method for selecting frame encoding parameters to improve transmission ...

US Pat. 6882634 - Filed Apr 4, 2001 - Broadcom Corporation
If a **jitter clock** is used for the sampling of the input **signal**, ... frame on an HPNA V2 network has three major components: **serialization** delay (the time it ...

Variable delay element for **jitter** control in high speed data links

US Pat. 6404257 - Filed May 30, 2000 - International Business Machines Corporation
A method for decreasing the amount of **jitter** present at the receiver input of ... and timing information for said skewing and **serialization** with said **clock** ...

Method for selecting an operating mode for a frame-based communications network

US Pat. 6888844 - Filed Apr 4, 2001 - Broadcom Corporation
If a **jitter clock** is used for the sampling of the input **signal**, ... frame on an 60 HPNA V2 network has three major components: **serialization** delay (the time ...

Method of determining a start of a transmitted frame in a frame-based ...

US Pat. 6993101 - Filed Apr 4, 2001 - Broadcom Corporation

If a **jitter clock** is used for the sampling of the input **signal**, ... frame on an HPNA V2 network has three major components: **serialization** delay (the time it ...

Time division multiplex data recovery system using close loop phase and ...
US Pat. 6901126 - Filed Jun 30, 2000 - Texas Instruments Incorporated
A Wizard port performs the data **serialization**, deserialization, and **clock** extraction functions for a physical layer interface device. ...

Method of enhancing network transmission on a priority-enabled frame-based ...
US Pat. 6954800 - Filed Apr 4, 2001 - Broadcom Corporation
If the input **signal** is a sinusoidal **signal** A*cos(wot), then the effect of the **jitter clock** is the 5 same as the input were A*cos |WO(T+K*sin(WT)}. ...

Serial-link circuit including capacitive offset adjustment of a high-speed ...
US Pat. 6728240 - Filed Feb 4, 2000 - The Board of Trustees of the Leland Stanford Junior University
Also, the **clock** load and hence **clock** buffer area, power and **jitter** are ...
In this circuit, a 1 ghz **clock signal** CLK and its mv of offset in 8 mv steps. ...

Method of controlling data sampling clocking of asynchronous network nodes ...
US Pat. 6975655 - Filed Apr 4, 2001 - Broadcom Corporation
Similarly, in the DAC data path, the **jitter clock** also can be 15 modeled with the sawtooth **signal** at the output of the noise-shaping digital modulator. ...

Method for selecting frame encoding parameters in a frame-based ...
US Pat. 6988236 - Filed Apr 4, 2001 - Broadcom Corporation
If a **jitter clock** is used for the sampling of the input **signal**, ... frame on an HPNA V2 network has three major components: **serialization** delay (the time it ...

Method of maintaining frame synchronization in a communication network
US Pat. 5668811 - Filed Jun 7, 1995 - National Semiconductor Corporation
10, the riming can be synchronized with a 125 bits of information (on average, conveying 4 bits of data and microsecond reference **clock signal** 214. ...

Method of determining a collision between a plurality of transmitting ...
US Pat. 6898204 - Filed Apr 4, 2001 - Broadcom Corporation
Similarly, in the DAC data path, the **jitter clock** also can be modeled with ... an HPNA V2 network has three major components: **serialization** delay (the time ...

Extended host controller **test** mode support for use with full-speed USB devices
US Pat. 7225288 - Filed Dec 20, 2002 - Advanced Micro Devices, Inc.
7 illustrates a low speed mode example where the data **signal** line and the ... **test** packet period, 14 **clock** cycles are needed to transmit the **test** pattern. ...

Built-in self **test** for speed and timing margin for a source synchronous IO ...
US Pat. 6760873 - Filed Mar 23, 2001 - LSI Logic Corporation
The input sequences go into the **serialization** logic 98 and the data output ...
These include the ASIC core **clock jitter** and duty cycle distortion, ...

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◉ Return patents filed between Jan 1970 and Feb 2003

Patents

Patents **1 - 8** on **serialization clock jitter "FIFO"**. (**0.14** seconds)

Sort by relevance | Sort by date (new first) | Sort by date (old first)

Asynchronous **serialization**/deserialization system and method
US Pat. 6140946 - Filed Jun 12, 1998 - International Business Machines Corporation
The bus controller 14 is connected to the resynchronized **clock**, due to the well-known **jitter** phenom- micro-controller core 10 via a processor bus 8, ...

Low pin count (LPC) I/O bridge
US Pat. 6990549 - Filed Nov 9, 2001 - Texas Instruments Incorporated
The internal **serialization clock** is frequency locked to the reference **clock** ...
The duty cycle should be not greater 45 than 40/60 and **jitter** should be less ...

High speed serial interface between image enhancement logic and ros for ...
US Pat. 5572721 - Filed Dec 13, 1994 - Xerox Corporation
This invention offers a solution to the high speed data **serialization** ...
circuits (eg the bitmap) are shown arriving at the **FIFO** 12 which stores them and ...

Synchronous collaboration based on peer-to-peer communication
US Pat. 6898642 - Filed Apr 17, 2001 - International Business Machines Corporation
The peer-to-peer, timestamp- and priority-based **serialization** protocol of ...
In the case of a **clock jitter** on a client, the **jitter** will tend to cause the ...

Data transmitter with sequential **serialization**
US Pat. 6665360 - Filed Dec 20, 1999 - Cypress Semiconductor Corp.
The transceiver device 220 may also, in one example, comprise a **FIFO** 222, ...
By reducing the **jitter** of the transmitter 100, the transceiver may be more ...

Timing synchronization methods and systems for transmit parallel interfaces
US Pat. 6977980 - Filed Aug 29, 2001 - Rambus Inc.
Other implementations have attempted to use **FIFO** or flip flop pairs. ...
can tolerate most timing variations due to **clock** path mismatches and **clock jitter**. ...

System and method for determining on-chip bit error rate (BER) in a ...
US Pat. 7093172 - Filed Nov 8, 2002 - Broadcom Corporation
Each lane assignment **FIFO** 322 may have a corresponding read and write pointer.
... for example, 64-bit data to 66-bit data for more efficient **serialization**. ...

System for transporting sub-rate data over a communication network
US Pat. 7110396 - Filed Aug 20, 2001 - CIENA Corporation
... data streams using local **clock** signals and to minimized data latency. ...
shape and **jitter** pattern as when these data streams were received at the ...

serialization clock jitter "FIFO" Search Patents

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Patents

Patents **1** - **2** on **serialization clock jitter test signal interpolator**. (**0.23** seconds)

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Did you mean: ***serialization clock jitter test signal interpolation***

Self **test** of an electronic device

US Pat. 6397042 - Filed Mar 2, 1999 - Texas Instruments Incorporated
The 35 frequency offset phase **interpolator** is still used on the transmit PLL, ... device comprising: a **clock** source, having an output for a **clock signal**; ...

Time division multiplex data recovery system using close loop phase and ...

US Pat. 6901126 - Filed Jun 30, 2000 - Texas Instruments Incorporated
The receivers 44 each trigger on only the rising edge of the **clock** to alleviate duty cycle issues. Aphase **interpolator** 44 tracks the received data **signal** ...

serialization clock jitter test signal interpolator Search Patents

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